Monolithic D/A Improves Conversion Times

With all npn transistors used for switching, self-adjusting inputs and 4-bit partitioning, this design brings new performance figures to monolithic D/A converters.

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Current switching techniques have largely replaced voltage switching in D/A conversion during the past 2 years. This removes the speed limitation imposed by charge storage of saturated, voltage switching transistors. Conversion speed is then limited by the transistor junction capacitances rather than the time delay common to saturated switching. However, as will be described, the basic current switching approach introduces a new stored charge delay as well as added linearity error. Both of these limitations have been removed by Burr-Brown engineers in their design of a monolithic D/A switch circuit that provides D/A conversion having 12-bit accuracy with 200-ns settling time to 1/2 LSB.

Avoid the Monolithic pnp

Settling time limitations of the basic current switching technique are primarily those imposed by the emitter-base and collector-base capacitances of the current source transistors. This basic technique is represented by an all npn circuit (Fig. 1) chosen to avoid the response problems of monolithic pnp transistors. Current sources formed by the lower transistors shown supply binary weighted currents to the output resistor R_L. These current sources are digitally controlled through the upper emitter-follower transistors and their level shifting zener diodes. When the high level of a logic signal is applied to one of the emitter-follower bases, it pulls the associated current source emitter to a higher voltage and turns it off.

In reverse biasing the emitter-base junction of a current source, the emitter-follower charges the capacitance of this junction. The charge so stored must be removed before the current source can be turned on again by a low logic level. However, the low logic level at the emitter-follower

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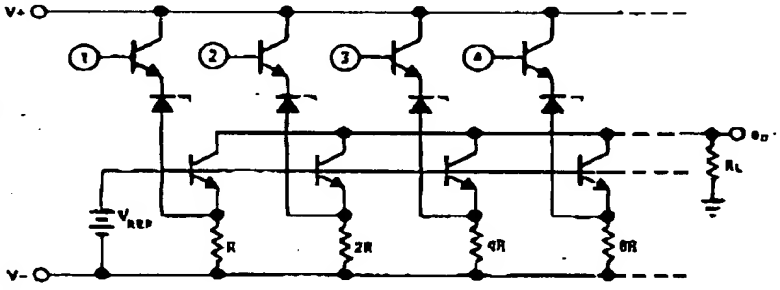

Fig. 1 – Basic D/A converter with npn transistors.

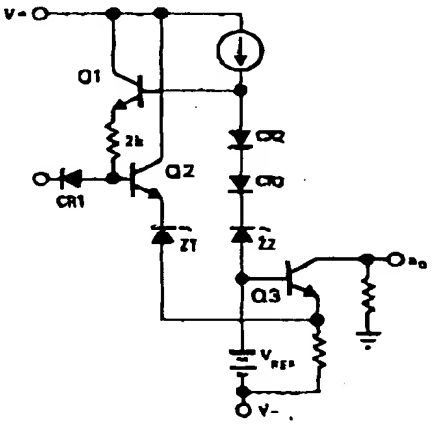

Fig. 2 – D/A current switch with charge control gating.

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base reverse biases this input transistor so the charge cannot be removed through the low impedance path which supplied it. Instead, the emitter-base capacitance must discharge through the much larger resistor connected in series with the emitter. As a result, the current source turn on is far slower than its turn off. While this current switching has avoided the charge storage delay of saturated operation, an equally serious delay is developed by charging the large emitter-base capacitance.

Optimize Stored Charge

Obviously then, switching time and the settling time in D/A conversion can be dramatically improved by limiting charge storage on these junction capacitances. The optimum level of stored charge is that which can be transferred to the emitter-base junction of the associated emitter-follower when that transistor turns off. In this way, no charge must be dissipated during switching. Rather, the stored charge is simply transferred back and forth between the two transistors. Assuming equal junction capacitances for the two transistors, equal and opposite changes in stored charge are produced by opposite voltage changes on these capacitances. Thus, the emitter-base voltage of the current source should be reduced to zero for turn off to match the voltage increase on the emitter-follower junction as it turns on.

However, the high logic level will not be consistent enough to insure a current source turn off drive that accurately reduces emitter-base voltage to zero. For TTL the high level output can drop from 4.5V to approach 2.5V depending upon fan out. If switch biasing permits turn off with the 2.5V level, then the 4.5V level applies a 2V overdrive to the current source emitter-base capacitance. To prevent this speed killing overdrive the inputs might be clamped, but this would draw excessive currents from the logic outputs.

Self-Adjusting Inputs

Instead, Burr-Brown developed a self-adjusting input gating circuit that controls the turn off drive independent of logic level and bias level variations. The gating circuit is shown in Fig. 2 with a single current switch. In this case the voltage applied to the base of the input emitter-follower, Q_2, is controlled by the input gate CR1 and its bias voltage as set by the emitter of Q_1. When the low logic level is applied at the input, CR1 conducts and holds the base of Q_2 at a voltage that is one diode drop above the input voltage. As the input voltage rises, the base voltage of Q_2 follows until Q_1 catches it. The maximum base voltage of Q_2 is limited to that fixed by Q_1, and no input overdrive can be transmitted to the current source Q_3. An input overdrive merely reverse biases the input gate CR1 which disconnects the input emitter-follower from the input signal. Note that this also unloads the logic output at the high level as is desirable.

Then by appropriate choice of the gating voltage limit of Q_1, the turn off voltage drive applied to the cur-

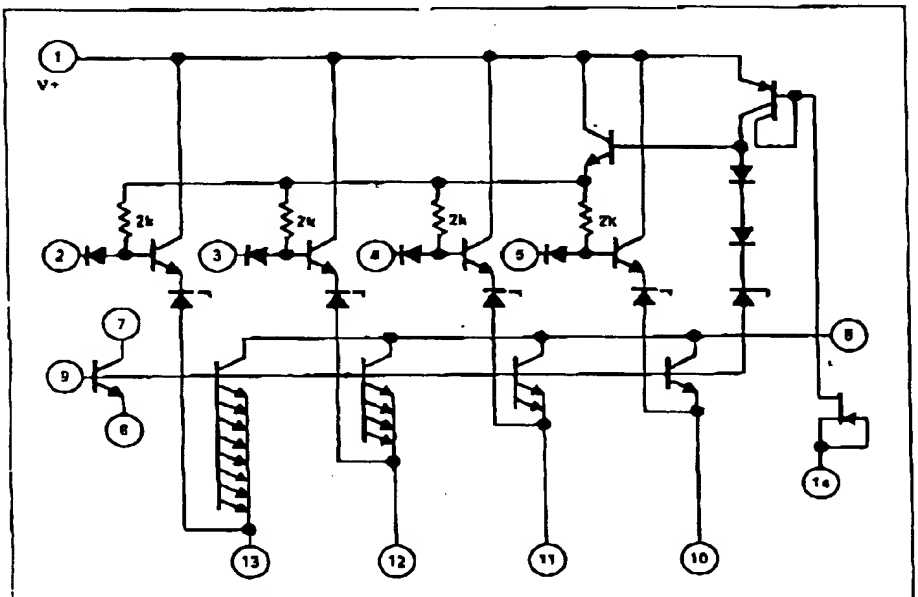

Fig. 3 – Schematic of the complete 4-bit monolithic D/A current switch.

rent source emitter-base junction can be optimized. As discussed, the emitter-base voltage in the off state should be zero for best switching speed. To insure this condition the limit voltage established by Q_1 must be adjusted for process and thermal variations in the voltages on Z_1 and Q_2. The limit voltage is made self-adjusting by deriving it from compensating voltages on Z_1 and CR3. Similarly, the voltage drop of CR2 compensates for that of the emitter-base junction of Q_1. As a result of this compensated biasing, the turn off voltage transmitted to Q_3 is consistently that needed for optimum switching speed.

Partitioning Helps, Too

The remaining response limitations and the major linearity error of current switching D/A conversion are largely removed by partitioning. As indicated in Fig. 3, each monolithic circuit includes only four bits. Additional bits are handled by identical quads whose output currents are weighted with scaling networks. Each quad internally conducts the same currents as the others, avoiding the extreme range of current levels common without the output scaling. This avoids a similar wide range of emitter resistors for which relative matching and tracking are poor. Also, currents do not range down to the low levels which reduce speed. The speed limitation imposed by the collector-base capacitances of the current sources can be avoided by supplying the output current to an op amp summing junction. In this way, the current source output voltages are constrained to very small changes by the op amp. This essentially eliminates the voltage swings on the collector-base capacitances and the associated speed reduction.

Match Emitter Current Density

Greater accuracy is achieved with the quad partitioning from the improved transistor matching it affords. By using multiple emitters on the current sources (Fig. 3), the current density in each emitter is made to match that of the emitters of the other transistors. The emitter-base voltages and betas of all current sources are then matched in spite of an 8:1 range in current levels. This approach is feasible because of the limited range of currents of the quad.

By means of its input gating circuit and its 4-bit partitioning, this design permits both high speed and high resolution in D/A conversion. While still providing 12-bit resolution, the switch achieves a 0.01% (1/2 LSB) settling time of 200 ns as compared to the 1.8 μs of similar quad switches. The design techniques discussed have been implemented into the Burr-Brown 4550 D/A switch. ▭

Jerald Graeme has been with Burr-Brown Research for 5 years where he now is manager of monolithic engineering. In this position Graeme directs the development of monolithic products and components. He holds a B.S.E.E. from the University of Arizona, an M.S.E.E. from Stanford University, has been granted two patents and is a member of IEEE and Tau Beta Pi.

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